

Attorney Docket No.: 00CON159PC-CIP4

**In the Claims:**

**Claim 1 (currently amended):** A structure comprising:

a substrate having a top surface and a bottom surface;

a first semiconductor die and a second semiconductor die attached to said top surface of said substrate, wherein said first semiconductor die is coupled both to said second semiconductor die and to said substrate;

a first heat spreader and a second heat spreader attached to said bottom surface of said substrate;

a first via and a second via in said substrate;

said first via providing a connection between said first semiconductor die and said first heat spreader, said second via providing a connection between said second semiconductor die and said second heat spreader.

**Claim 2 (original):** The structure of claim 1 wherein said first and second heat spreaders are attached to a printed circuit board.

**Claim 3 (original):** The structure of claim 1 further comprising a first substrate down bond area attached to said top surface of said substrate, wherein said first via provides an electrical connection between said first substrate down bond area and said first heat spreader.

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**Claim 4 (original):** The structure of claim 3 wherein a first semiconductor die ground bond pad on said first semiconductor die is electrically connected to said first substrate down bond area by a first down bonding wire.

**Claim 5 (original):** The structure of claim 1 wherein a third via in said substrate provides a connection between a first signal bond pad of said first semiconductor die and a printed circuit board.

**Claim 6 (original):** The structure of claim 1 wherein said substrate comprises organic material.

**Claim 7 (original):** The structure of claim 6 wherein said organic material is selected from the group consisting of polytetrafluoroethylene material and an FR4 based laminate material.

**Claim 8 (original):** The structure of claim 1 wherein said substrate comprises a ceramic material.

**Claim 9 (original):** The structure of claim 5 wherein said third via provides an electrical connection between a first substrate bond pad and said printed circuit board, wherein said first substrate bond pad is electrically connected to said first signal bond pad of said first semiconductor die.

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**Claim 10 (original):** The structure of claim 9 wherein said first substrate bond pad overlaps said third via.

**Claim 11 (original):** The structure of claim 9 wherein said first substrate bond pad is electrically connected to said first signal bond pad of said first semiconductor die by a first signal bonding wire.

**Claim 12 (original):** The structure of claim 5 wherein said third via provides an electrical connection between said first signal bond pad of said first semiconductor die and a first land, said first land being electrically connected to said printed circuit board.

**Claim 13 (original):** The structure of claim 12 wherein said third via overlaps said land.

**Claim 14 (currently amended):** A structure comprising:

- a substrate having a top surface and a bottom surface;
- a first semiconductor die and a second semiconductor die attached to said top surface of said substrate, wherein said first semiconductor die is coupled both to said second semiconductor die and to said substrate;
- a heat spreader attached to said bottom surface of said substrate;
- a first via and a second via in said substrate;

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said first via providing a connection between said first semiconductor die and said heat spreader, said second via providing a connection between said second semiconductor die and said heat spreader.

**Claim 15 (original):** The structure of claim 14 wherein said heat spreader is attached to a printed circuit board.

**Claim 16 (original):** The structure of claim 14 further comprising a first substrate down bond area attached to said top surface of said substrate, wherein said first via provides an electrical connection between said first substrate down bond area and said heat spreader.

**Claim 17 (original):** The structure of claim 16 wherein a first semiconductor die ground bond pad on said first semiconductor die is electrically connected to said first substrate down bond area by a first down bonding wire.

**Claim 18 (original):** The structure of claim 14 wherein a third via in said substrate provides a connection between a first signal bond pad of said first semiconductor die and a printed circuit board.

**Claim 19 (original):** The structure of claim 18 wherein said third via provides an electrical connection between a first substrate bond pad and said printed circuit board,

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wherein said first substrate bond pad is electrically connected to said first signal bond pad of said first semiconductor die.

**Claim 20 (original):** The structure of claim 19 wherein said first substrate bond pad overlaps said third via.

**Claim 21 (original):** The structure of claim 19 wherein said first substrate bond pad is electrically connected to said first signal bond pad of said first semiconductor die by a first signal bonding wire.

**Claim 22 (original):** The structure of claim 18 wherein said third via provides an electrical connection between said first signal bond pad of said first semiconductor die and a first land, said first land being electrically connected to said printed circuit board.

**Claim 23 (original):** The structure of claim 22 wherein said third via overlaps said land.